*International Journal of Latest Trends in Engineering and Technology*
*Vol.(10)Issue(3), pp.208-214*
*DOI: http://dx.doi.org/10.21172/1.103.36*
*e-ISSN:2278-621X*

# DESIGN AND IMPLEMENTATION OF 3-BIT FLASH ANALOG TO DIGITAL CONVERTER (ADC)

Prof. Jayashree C Nidagundi[1], Sunita S Bettakusugal[2]

**Abstract: Analog to Digital converters are essential in all communication and signal processing applications. Among all ADC'S Flash ADC has a high speed conversion rate. It has a capacity of sampling a signal up to Giga Bites. The conventional Flash ADC contains the resistor ladder network, comparator, and encoder. Due to the use of resistor ladder network in conventional Flash ADC static power consumption is more to overcome this issue, new 3-Bit Flash ADC has been proposed. The proposed ADC is consists of sample and hold (S/H) circuit, threshold modified comparator circuit and priority encoder. The design is implemented using cadence virtuoso schematic tool under cadence 180nm Technology with a supply voltage of 1.8 V and clock frequency of 1M Hz. Simulation is carried using cadence spectre simulator tool.**
**Keywords - ADC, sample and hold(S/H) circuit, TMCC, Threshold voltage, Multiplexer, encoder and Flash ADC.**

## 1. INTRODUCTION

Now a days, the demand for portable battery operated devices are goes on increasing, For high speed applications the researchers are mainly concentrating on low power consumption Devices such as low power analog to digital converters (ADC), Analog to Digital converters are most important functional units in the signal processing , system on chip(soc) and mixed signal design applications [4].

Analog to Digital Converter (ADC) is a system that converts analog signal into digital signal that is zeros and ones, such as a sound picked up by a microphone or light entering a digital camera into digital values is 0's and 1's. An ADC may contains an electronic gadget that converts an input Analog voltage or current into a digital number representing the magnitude of the voltage or current. Different ADC architectures are available for different purposes. Due to the complexity and the accurately coordinated with other components, all but the mostly specialized ADCs are implemented as integrated circuits (ICs).

Designing and testing of analog circuits is very difficult compared to digital circuits.The Storage of analog circuits also very complex. Therefore to process and storage analog circuits are converted into digital form. ADC's are used to convert a analog signal into digital signal in terms of 0's and 1's. The performance of ADC depends mainly on resolution, sampling rate and power consumption. Analog circuits are commonly used in more power constrained situations. The power consumed by a digital CMOS logic is directly proportional to square inverse of the scaling factor (k).

$$Digital\ power \propto k-2 \quad .....1$$

On the other hand, analog power consumed by CMOS Flash ADC scales with the inverse of a scaling with the inverse of a scaling factor when bandwidth is held constant.

$$Analog\ Power \propto k-1 \quad .....2 \quad [6]$$

Organisation: section 2 consists of conventional Flash ADC architecture, Proposed Architecture is covered in section 3, In section 4, the implementation details and results discussion, Section 5 concludes paper.

## 2. CONVENTIONAL FLASH ADC ARCHITECTURE

A Flash ADC is a type of analog-to-digital converter. Compared to the all ADC's the Flash ADC performs the conversion at very high speed and is capacity of sampling rate up to Giga bites. The conventional Flash ADC consists of comparator bank, resistive ladder network and digital encoder, it is shown in figure 1. For n-bit ADC $2^n$-1 comparators are used. The resistive ladder network is the set of resistors, it acts as a voltage divider and it produces reference voltages to the comparator. Comparator is an important component in Flash ADC, which converts the analog signal into digital signal [2]. Each comparator compares the input voltage Vin with the reference voltages Vref. If the input voltage is greater than the reference voltage the output of comparator goes high, if input signal is less than the reference voltage the output of a comparator is low [13]. The outputs produced by a comparator is a thermo codes, which resembles the output produced by a thermometers. Different types of comparators are available. The thermo codes are converted into binary codes using digital encoder.

[1] Assistant Professor in Department of Electronics and Communication, S.D.M .College of Engineering and Technology, Dharwad, India.
[2] Department of Electronics and Communication, S.D.M .College of Engineering and Technology, Dharwad, India.

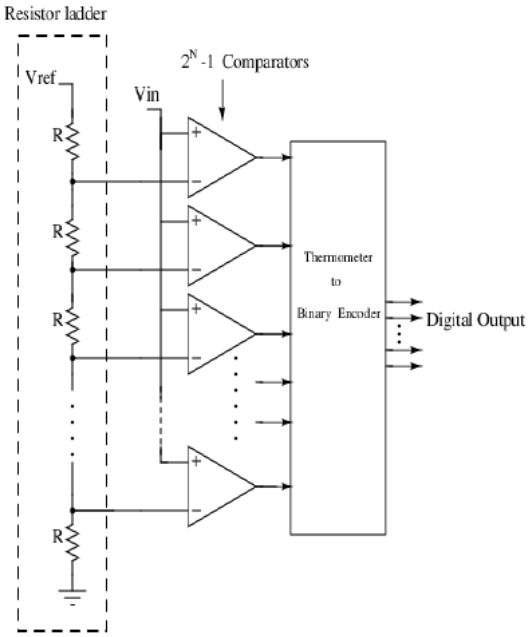



Figure 1: Conventional N-bit Flash ADC

**3. RELATED WORK**

As per the literature survey [1], 3-bit Flash ADC is implemented in 130nm technology. Threshold inversion quantisation modified comparator circuit is used. The TIQ based comparator technique reduces non linearity in case of process variations. In [2], a low power 5-bit hybrid flash architecture is proposed mainly for low power application. The proposed analog to digital converter is the combination of both conventional double-tail comparators and standard cell comparators. The main disadvantage of flash ADC is that it need large area and dissipate large amount of power. To overcome this complexity,The numbers of comparators are reduced by using Threshold Modified Comparator circuit and multiplexer based encoder [3]. In [4] a new architecture implementation for the 4-bit flash ADC is proposed. The design is suitable for low power high-speed applications. The architecture uses threshold quantization technique (TIQ) and the Pseudo- dynamic NMOS. In [6], 4-bit Flash ADC is designed using TMCC comparator and Rom encoder. The TMCC comparators are designed to optimize the input offset voltages by systematically and consistently varying the. In [7], In this paper converter is designed using variable threshold voltage CMOS comparator and a Xor based encoder circuit. The ADC is designed and analyzed by Cadence Virtuoso Analog Design Environment using UMC 180nm technology.

**4. PROPOSED ARCHITECTURE**

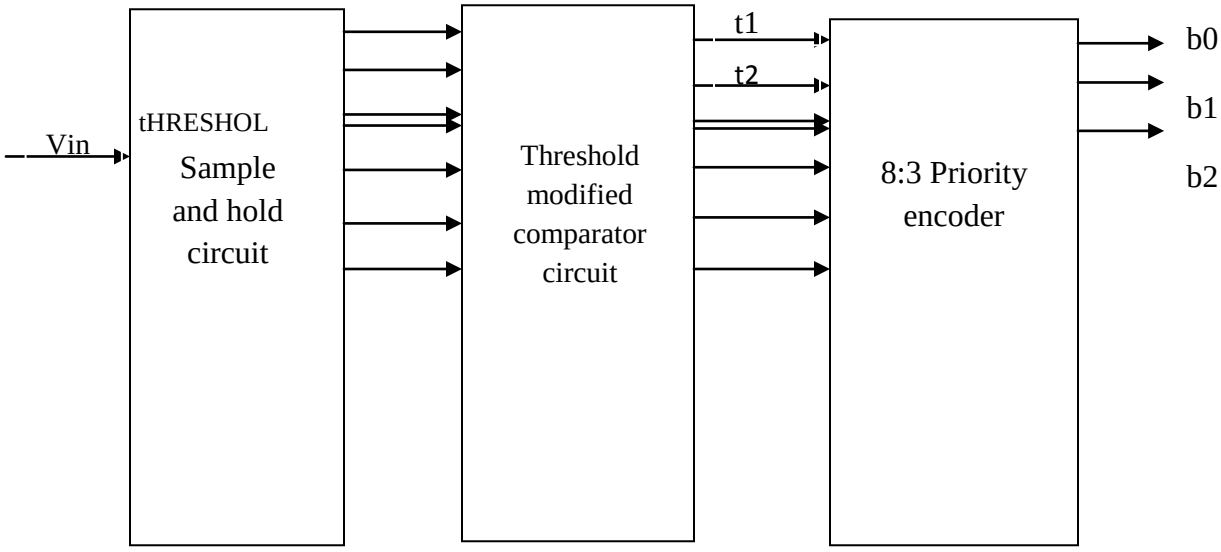



Figure 2: Proposed 3-bit Flash ADC

The proposed 3-bit Flash ADC is shown in the Figure 2. It consists of a sample and hold (S/H) circuit, threshold modified comparator circuit (TMCC) and priority encoder. Sample and hold (S/H) circuit is used to convert the analog signal into digital signal, the output produced by S/H circuit is quantized one. The output of S/H is fed as a input to the Threshold Modified Comparator Circuit (TMCC). S/H circuit samples the input signal at a specified period of time based on the clock signal. The TMCC is a double cascaded inverter circuit. TMCC compares the input voltage and a reference voltage and produces thermometer codes. The width and length of the first inverter is changed to calculate the threshold voltage. The output produced by a comparator is similar to the codes generated by a thermometer. For n-bit converter $2^n$-1 TMCC's are used. The output of comparator is given as a input to the priority encoder that converts thermometer codes into binary codes based on the highest priority. For 3-bit Flash ADC 8:3 priority encoder is used.

*4.1 Sample and Hold circuit:*

A S/H circuit is an analog device that holds the sampled value for a predetermined time at a consistent level, and it samples the voltage of a continuously varying analog signal [9]. Sample and hold circuits are used in linear systems. The simplest S/H circuit in MOS technology is shown in Figure 3, where Vin is the input signal, M1 is an MOS transistor operating as the sampling switch, Cs is the hold capacitor, ck is the clock signal, and Vout is the resulting sample-and-hold output signal.

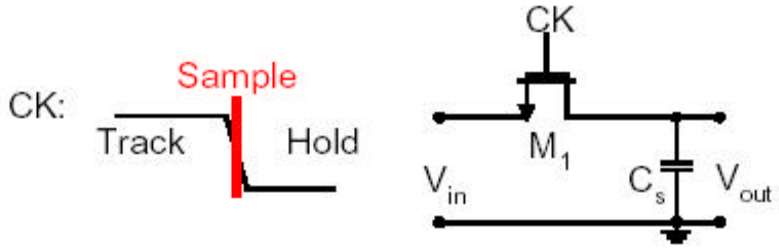



Figure 3: Sample and Hold circuit

The operation of this circuit is very straightforward. Whenever ck is high, the MOS switch is on, which in turn allows Vout to track Vin. On the other hand, when ck is low, the MOS switch is off. During this time, Ch will keep Vout equal to the value of Vin at the instance when ck goes low.

*4.2 Threshold Modified Comparator Circuit (TMCC)*

Due to the use of resister ladder circuit static power consumption and delay of comparator is more. To reduce the delay and power consumption TMCC is used. The TMCC comparators are designed to optimize the input offset voltages by systematically and consistently varying the transistor sizes of the differential transistor pair. TMCC is basically a buffer circuit consisting of an inverter with modified threshold voltage followed by a NOT gate as depicted in Figure 4 [3].

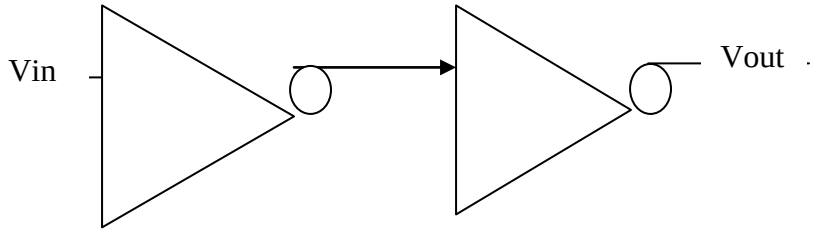



Figure 4: Threshold Modified Comparator Circuit

For an inverter present in TMCC when the input voltage is less than threshold (reference) voltage the pull-up transistor is ON and pull-down transistor will be OFF thereby providing a high output considered as logic 1. But when the input is more than threshold, pull-down transistor will come into ON state thereby giving a low output interpreted as logic 0. If we focus the operation phenomena of a comparator it is quite opposite to that of a comparator. TMCC is a cascaded connection one NOT gate with the inverter to The main advantage of inclusion of NOT gate serves the purpose of logic restoration of the output of an inverter circuit [3].

According to the reference voltage calculated from potential divider network of usual flash ADC, the width length ratio of the MOS transistors used in the inverter circuit of TMCC are altered so as to get the modified threshold voltage. The relation between threshold voltage and the aspect ratio can be given by the following equation [6];

$$Vth = \frac{vto,n+\sqrt{1/kr(vdd+vto,p)}}{1/kr} \quad \text{.....} \quad (3)$$

Where as

$$Kn = \mu n.Cox.(W/L)n \quad \text{.....} \quad (4)$$

$$Kp = \mu m.Cox.(W/L)p \ldots\ldots \quad 5$$

And the trans conductance ratio,

$$Kr = Kn/Kp = \frac{\mu n\left(\frac{W}{L}\right)n}{\mu\, p\left(\frac{W}{L}\right)P} \ldots\ldots\ldots \quad 6$$

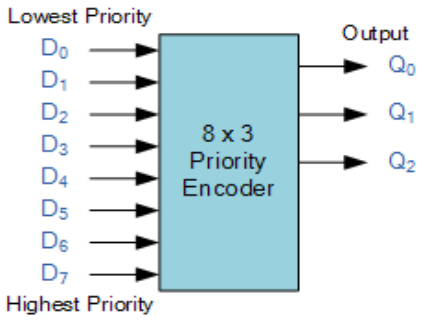
The aspect ratios of each comparator are adjusted using the dc analysis. The theoretical and practical values, threshold voltages and aspect ratio is shown Table 1.

Table I: Variable threshold voltages of TMCC

| Theoretical comparator values in volts(v) | Practical values in volts(v) | Width of pmos | Length of pmos | Width of Nmos | Length of Nmos |
|---|---|---|---|---|---|
| 0.225 | 0.281 | 400n | 10u | 50u | 300n |
| 0.45 | 0.451 | 900n | 200n | 48u | 200n |
| 0.675 | 0.673 | 20u | 180n | 38u | 180n |
| 0.9 | 0.899 | 10u | 180n | 3u | 180n |
| 1.125 | 1.13 | 26u | 180n | 1u | 180n |
| 1.35 | 1.36 | 15u | 180n | 420n | 10u |
| 1.575 | 1.45 | 50u | 180n | 400n | 20u |

*4.3. Priority Encoder*

Priority Encoder is a circuit or algorithm that constricts several inputs into lesser number of outputs. The output of the priority encoder is the binary portrayal of the primary numbers beginning from zero of the most significant input bit. They are ofttimes utilized to control interrupt requests by acting on the highest priority encoder. If two or more inputs are fed in a mean time, the input having the highest priority will take the precedence. For example Inputs D2 (010), D3 (011) and D5 (101) are send simultaneously, and all are having the highest priority. Out of three inputs the D5 has a highest priority so it will directly fed at the output side. Hence the output becomes 101.




| Inputs | | | | | | | | Outputs | | |
|---|---|---|---|---|---|---|---|---|---|---|
| $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | $Q_2$ | $Q_1$ | $Q_0$ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | x | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 1 | x | x | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 1 | x | x | x | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | x | x | x | x | 1 | 0 | 0 |
| 0 | 0 | 1 | x | x | x | x | x | 1 | 0 | 1 |
| 0 | 1 | x | x | x | x | x | x | 1 | 1 | 0 |
| 1 | x | x | x | x | x | x | x | 1 | 1 | 1 |

Figure 5: Block diagram and Truth table

## 5. RESULTS AND DISCUSSION

*Schematic of 3-bit ADC*

ADC is a cascaded connection of S/H Circuit, TMCC and a priority encoder as shown in figure 15. The output of sample and hold circuit is fed as input to the TMCC. Threshold modified comparator circuit produces thermometer codes. These codes are converted into binary codes using priority encoder.

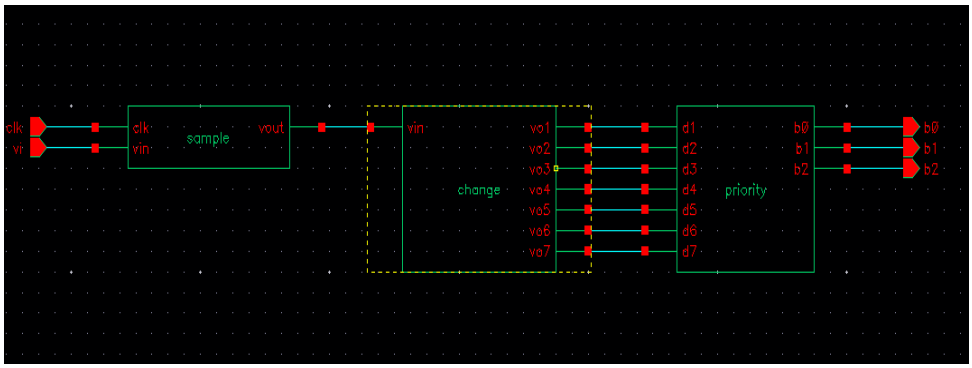



Figure 6: Schematic of 3-bit ADC

*5.1 Symbol of 3-bit ADC*

Symbol is created after the schematic design step. The analog input frequency is 1 MHz with supply voltage of 1.8 V and amplitude of 2V with carrier signal having amplitude of 5 V with frequency of 10M Hz.

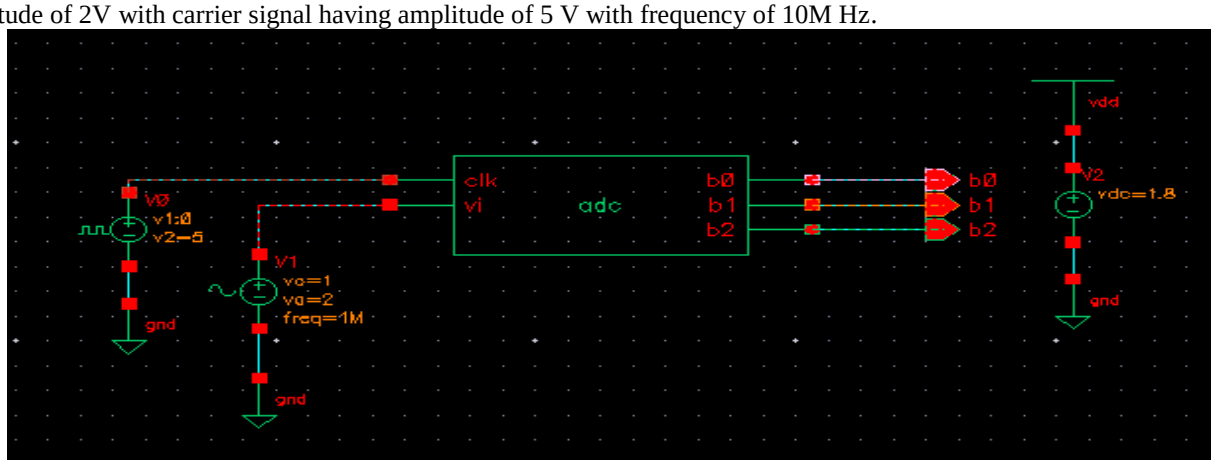



Figure 7: Symbol of 3-bit ADC

*5.2 Transient analysis of 3-bit ADC*

The proposed ADC is simulated in cadence spectre simulator. For analog input voltage all digital codes are generated, starting from 000 to 111 it is show in Figure 17.

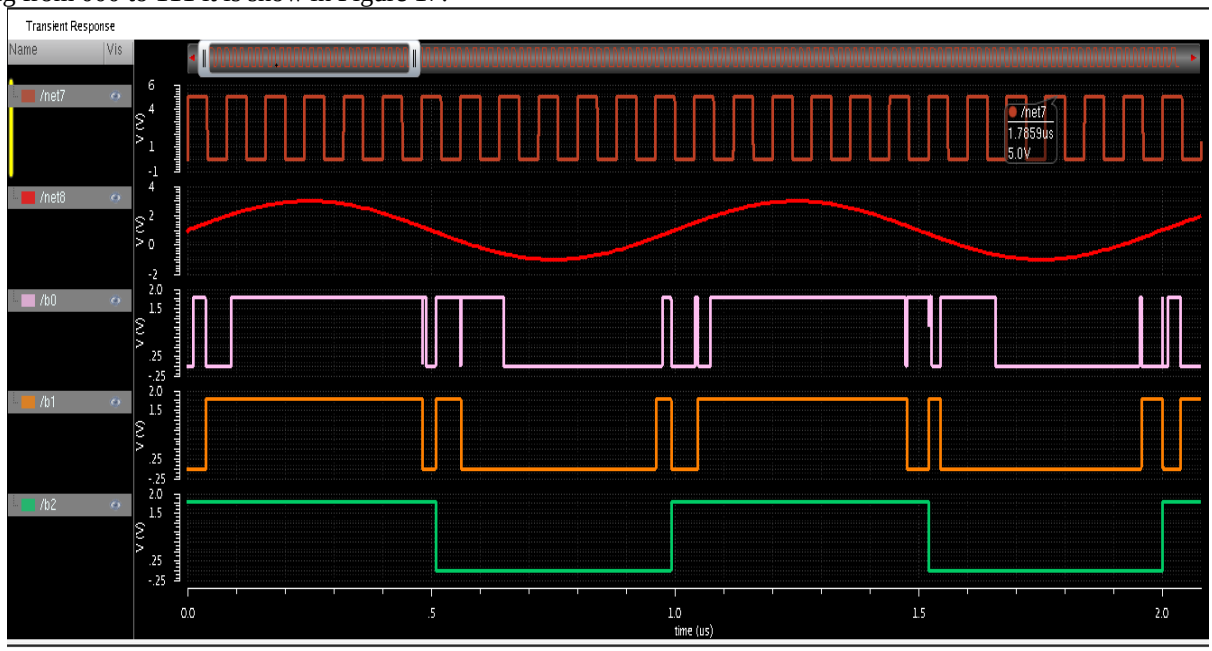



Figure 8: Transient analysis of 3-bit ADC

Table 2 : Truth Table of 3-bit ADC

| | | ADC OUTPUT | | |
|---|---|---|---|---|
| Input range Vin in V | Comparator Output | B2 | B1 | B0 |
| 0 <Vin< 0.225 | 0000000 | 0 | 0 | 0 |
| 0.225 < Vin < 0.45 | 0000001 | 0 | 0 | 1 |
| 0.45 < Vin < 0.675 | 0000010 | 0 | 1 | 0 |
| 0.675< Vin < 0.9 | 0000010 | 0 | 1 | 1 |
| 0.9 < Vin < 1.125 | 0000100 | 1 | 0 | 0 |
| 1.125 < Vin < 1.35 | 0001000 | 1 | 0 | 1 |
| 1.35 < Vin < 1.5 | 0100000 | 1 | 1 | 0 |
| Above 1.5 | 1000000 | 1 | 1 | 1 |

*5.3 Power Dissipation of ADC's*

Table 3: Comparison of Power Dissipation of ADC's

| Paper No | Power consumption in mW | Resolution in bits | Types of comparator used |
|---|---|---|---|
| [2] | 7.1 | 5-bits | Double tail and standared cell comparator |
| [4] | 1.98 | 4-bits | Threshold inverter quantization type comprator |
| [5] | 6.4 | 4-bits | Comparators with multiplexers |
| [6] | 4.3 | 4-bits | TMCC and NOR ROM based encoder |
| [7] | 6.21 | 4-bits | Differential comparator |
| [8] | 7.84 | 4-bits | New proposed comparator and priority encoder |
| [9] | 1.05 | 3-bits | Preamplifier latch based comparator |
| [10] | 36.78 | 3-bits | Low power comparator and Nor based encoder |
| Proposed architecture | 0.345 | 3-bits | TMCC and priority encoder |

## 6. CONCLUSION

The proposed Flash ADC is designed by utilizing Sample and Hold circuit, Threshold Modified Comparator Circuit (TMCC) and Priority Encoder. The S/H circuit is utilized for transformation of analog signal to digital signal, The TMCC produces the thermometer codes and encoder changes over the thermometer codes into parallel codes based on priority. The power consumption is very less due to the removal of resistor ladder network. The power consumed by a proposed architecture is 0.384 mW for 1 MHz input frequency with a supply voltage of 1.8 V. The implementation is done cadence GPDK 180nm technology. Dc and transient analysis done on cadence spectre simulator tool.

## 7. FUTURE SCOPE

Proposed Flash ADC is designed for 3-bit the design can be further extended to higher resolution bit. In the proposed Design threshold modified comparator is used, in future it can be designed by using any other types of comparators. In the proposed design priority encoder is used to converting thermometer codes into binary values, in future we can design ADC using different types of encoders.

## 8. REFERENCES

1. Swarupa B N, Dr. Vijaya Prakash A M, Kumaraswamy K V "Implementation of a 3-bit Flash ADC using TIQ Modified Comparator Circuit and NORROM based Encoder" International Journal of Innovative Research in Computer and Communication Engineering Vol. 5, Issue 5, May 2016.
2. Mayur. S. M, Siddharth R. K, Nithin Kumar Y. B, Vasantha M. H "Design of Low Power 5-bit Hybrid Flash ADC" 2016 IEEE Computer Society Annual Symposium on VLSI.
3. Aditi Kar, Alak Majumder Abir Jyoti MandaI & Nikhil Mishra "Design of Ultra Low Power Flash ADC using TMCC & Bit Referenced Encoder in 180nm Technology" IEEE 2015 International Conference on VLSI Systems, Architecture, Technology and Applications (VLSI-SATA).

4. Liyaqat Nazir, Burhan Khurshid and Roohie Naaz Mir "A 7GS/s, 1.2 V. Pseudo logic Encoder based Flash ADC Using TIQ Technique" IEEE INDICON 2015.
5. Mrs. Jasbir Kaur and Mr. Saurabh Kansal "A New Power and Area Efficient 4-bit Flash ADC Using Multiple Selection Method" International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE) Volume 4, Issue 7, July 2015.
6. Mr. K. N. Hosur, Mr. Dariyappa, Mr. Shivanand, Mr. Vijay, Mr. Nagesha, Dr. Girish V. Attimarad, and Dr. Harish "Design of 4-bit flash ADC using TMCC and Nor ROM encoder in 90nm technology" in 2015 IEEE.
7. Gulrej Ahmed & Rajendra Kumar Baghel "A Variable Threshold Voltage CMOS Comparator for Flash Analog to Digital Converter" International Journal of Computer Applications (0975 – 8887) Volume 88 – No.7, February 2014.
8. Prakruthi T.G Siva Yellampalli "Design and Implementation of Sample and Hold Circuit in 180nm CMOS Technology" 978-1-4799-8792-4/15/$31.00_c 2015 IEEE.
9. Arunkumar P Chavan Rekha G P Narashimaraja "An Efficient Design of 3bit and 4bit Flash ADC" in International Journal of Computer Applications (0975 – 8887) Volume 61– No.11, January 2013.
10. Pradeep Kumar and Amit Kolhe "Design & Implementation of Low Power 3-bit Flash ADC in 0.18µm CMOS" International Journal of Soft Computing and Engineering (IJSCE) ISSN: 2231-2307, Volume-1, Issue-5, November 2011.